# AN10721

## Logic level $V_{GS}$ ratings for NXP power MOSFETs

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### Document information

| Info | Content |
|---|---|
| **Keywords** | gate–source voltage, logic level, rating |
| **Abstract** | Explanation of the link between the absolute maximum rating of gate–source voltage ($V_{GS}$) for a logic level power MOSFET, the design maximum gate source voltage rating and the long-term reliability of the product. |

### Revision history

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| 01 | 20080718 | Initial release |

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## 1. Introduction

The aim of this applications note is to clarify the link between the absolute maximum rating of gate - source voltage ($V_{GS}$) for a logic level power MOSFET, the design maximum gate source voltage rating and the long-term reliability of the product.

## 2. Key points

- NXP data sheets are compiled based on the requirements of IEC60134 and JESD22A108.
- This application note applies to all 25 V and 30 V drain-source voltage ($V_{DS}$) rated NXP N channel power MOSFETs with $R_{DS(on)}$ quoted at a $V_{GS}$ of 4.5 V and 10 V, with an absolute maximum $V_{GS}$ rating of 20 V. Such parts are described as “Logic Level” and the gate rating letter in the part number will be “L”.
- The absolute maximum rating of the gate source voltage ($V_{GS}$) is 20 V. This is an absolute maximum condition that must not be exceeded within the lifetime of the product within the customer’s application. This rating is not intended as a guarantee of the reliability of the product up to the absolute maximum rating, (i.e. it does not infer any long-term capability) but as a guideline as to the level of applied voltage above which there is a risk of immediate damage to the product.
- The High Temperature Gate Bias (HTGB) reliability of these products has been verified using an applied $V_{GS}$ of 16 V (i.e. 80 % of the absolute maximum value) for 1000 hours at a temperature of 150 °C. This is the maximum operating voltage that a design engineer should consider when using these parts. Any excursions above this value should be limited to 20 V and be short and infrequent in nature (e.g. voltage spikes). These products should not be used if a gate drive voltage in excess of 16 V is to be applied to the device.
- This approach of performing gate bias life testing at 80 % of the absolute maximum rating is consistent with the relevant quality specifications and the approach of a number of competitors for this type of product. Most other NXP N channel power MOSFETs undergo gate bias life testing at 100 % of the absolute maximum rating.
- To ensure that all devices are compliant to the absolute maximum $V_{GS}$ rating and to ensure the reliability of the product, all NXP devices experience a short duration production test that applies a $V_{GS}$ greater than the absolute maximum $V_{GS}$ level. This test is carefully designed to filter out devices with weak gate oxides without damaging good devices. This is a standard test applied to NXP power MOSFETs to ensure the long term reliability of our products.
- Performing gate bias life tests at 80 % of the absolute maximum $V_{GS}$ rating is suitable for the applications in which the products covered by this application note will be used. For example, for applications such as a computer motherboard, the applied gate voltage will be either 5 V ± 5 % (4.75 V to 5.25 V less driver voltage drop, from ATX supply specification) or 12 V ± 15 % (10.2 V to 13.8 V less driver voltage drop, note that the ATX specification is tighter at 5 %). In this case, the gate driver voltage will be less than the 16 V life tested value.

## 3. Life testing constraints

When designing a power MOSFET technology there are two conflicting constraints with respect to the gate oxide thickness used in the technology. Achieving a low $R_{DS(on)}$ at a low applied level of $V_{GS}$ infers a thin gate oxide, whereas a high absolute maximum $V_{GS}$ rating infers a thick gate oxide. In most cases, both requirements can be met whereby gate bias life testing can be performed at a value of 100 % of the absolute maximum rating. However, there are some instances where this is not possible.

When logic level devices were first introduced they were designed to interface directly to 5 V logic. The devices were designed so that a guaranteed $R_{DS(on)}$ was quoted at 5 V and 10 V. The maximum gate rating was quoted at a $V_{GS}$ of 20 V and the device was life tested under that condition.

However, as these parts started to be used with bootstrap power supplies (e.g. high side MOSFET in a buck converter), customers required the $R_{DS(on)}$ to be guaranteed at 4.5 V to take into account the diode drop in the bootstrap circuit and also to account for the tolerance of the 5 V rail of the computer power supply. In order to guarantee the $R_{DS(on)}$ at 4.5 V a slightly thinner gate oxide is required. A consequence of this is that the maximum DC voltage that can be reliably applied to the gate is also reduced.

Since some customers still required an absolute maximum rating of 20 V to ensure that the device was not damaged by voltage transients of up to 20 V, gate bias testing was reduced to 80 % of the absolute maximum rating to ensure that the device was reliable for the DC gate drive voltages that the devices were expected to experience. In addition, gate oxide screening tests remained above 20 V and gate leakage tests at 20 V were still applied to ensure that the devices would withstand gate voltage transients up to the 20 V absolute maximum voltage level.

## 4. IEC and JEDEC standards conformance

### 4.1 JEDEC JESD22A108C section 4.2.3.4 High temperature gate bias (HTGB)

This section states:

“The HTGB test biases gate or other oxides of the device samples. The devices are normally operated in a static mode at, or near, maximum-rated oxide breakdown voltage levels. The particular bias conditions should be determined to bias the maximum number of gates in the device. The HTGB test is typically used for power devices.”

This allows 80 % of the rated maximum voltage to be used as the bias voltage for this test.

### 4.2 IEC60134 paragraph 4: Absolute maximum rating system

This section states:

“Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment."

This defines the worst case conditions and highlights the responsibility of the designer to ensure that the absolute maximum value is never exceeded. It does not explicitly place any obligations on the manufacturer in terms of long term reliability. The aim of this applications note is to clarify the link between the absolute maximum rating and the long term reliability of the product.

## 5. References

**[1]** **JEDEC JESD22A108C section 4.2.3.4** — High temperature gate bias (HTGB)

**[2]** **IEC60134 paragraph 4** — Absolute maximum rating system

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